In the Claims

Amend claims 1-16 as follows:

1. (Currently Amended) A memory system comprising:

a plurality of DRAMs having circuits to accept non-inverted input signals and inverted input signals;

a register programmed to provide inverted or non-inverted signals to the DRAMS; and

programmable pins in the register and the DRAMs to enable operation in either non-inverted or inverted mode, wherein ~~one~~ a first programmable pin is connected to ground to ~~provide one~~ enable an inverting mode and ~~the other~~ a second programmable pin is connected to Vdd to operate in ~~the other~~ a non-inverting mode.

2. (Original) The memory system of claim 1 which includes re-drive circuitry, which can output both non-inverted and inverted polarity signals from one or more input signals.

3. (Canceled)

4. (Previously Amended) The memory system according to claim 1 wherein the DRAMs are mounted on a DIMM.

5. (Canceled)

6. (Currently Amended) A memory system comprising:

a plurality of DRAMs having receiver circuits adapted to interface with a plurality of signal drivers capable of providing both non-inverted and inverted address and command signal polarities to the plurality of DRAMs; and

a memory controller capable of ~~configuring~~ enabling the plurality of DRAMs to accept either non-inverted or inverted signals using a programmable pin, which dynamically configures the polarities of address and command signals exchanged between a plurality of signal drivers and the plurality of DRAMs, such that simultaneous switching noise in the memory system is reduced.

7. (Canceled)

8. (Original) The memory system of claim 6 wherein the pin is hard-wired to the DRAMs.

9. (Original) A memory system of claim 1 in which the register drives either non-inverted or inverted signals to the DRAMs using a programmable pin.

10. (Previously Amended) A memory system comprising:

a module having a plurality of DRAMs with inputs and outputs and circuits to accept either non-inverted input signals and inverted input signals, wherein pre-selected DRAMs may operate in the inverted mode with some critical signals remaining in a non-inverted mode;

a means connected to the circuits for changing modes to accept inverted input signals; and

a memory controller which is programmable to operate in non-inverted mode at power up and to change after it is programmed.

11. (Canceled)

12. (Original) The memory system of claim 10 wherein the memory controller may operate in the inverted mode with some critical signals remaining in non-inverted mode.

13. (Original) The memory system of claim 10 wherein a programmable pin is hard-wired to the module.

14. (Original) The memory system of claim 10 wherein the means for changing modes includes a pin that is controlled by the memory controller.

15. (Previously Amended) A DIMM comprising:

a plurality of DRAMs with means for operating with non-inverted or inverted signals based on a pre-selected operating mode; and

signal re-drive circuitry adapted to invert an address or command input signal subsequently output to one or more of the plurality of DRAMs, wherein an output mode of the signal re-drive circuitry is responsive to a programmable input.

16. (Previously Amended) A computer system with a memory system comprising:

memory devices and re-drive circuitry external to the said memory devices, said re-drive circuitry adapted to invert an address or command input signal subsequently output to one or more of the plurality of DRAMs via a programmable input, such that simultaneous switching noise is reduced, wherein said memory devices are designed to operate with non-inverted or inverted signals based on a selected operating mode.

17. (New) A memory module, comprising:

a plurality of memory devices each having a plurality of programmable address and control inputs that are configured by a plurality of programmable pins each dedicated to one of the plurality of memory devices, such that the plurality of memory devices may be individually

programmed to receive non-inverting or inverting inputs; and

a plurality of registers integral to the memory module, each programmed to output to a corresponding one of the plurality of memory devices, at least a portion of received address and command signals as non-inverted or inverted in response to received address or command inputs, such that normal operation of the plurality of memory devices is maintained.